PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.:	10/035,401
Filing Date:	December 28, 2001
Applicant:	Yat-Tung Lam
Group Art Unit:	2627
Examiner:	Glenda P. Rodriguez
Title:	RACE AVOIDANCE IN DISK HEAD READ CIRCUIT
Attorney Docket:	MP0056.C1

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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Applicant requests Pre-Appeal Brief Review and contend that Kuroda (U.S. Patent No. 6,522,608) fails to teach or suggest the elements of the presently pending claims.

STATUS OF CLAIMS

Claims 7, 13, 20, 29, and 36 are objected to. Claims 1, 2, 6, 8, 12, 14, 15, 19, 23, 24, 28, 30, 31, and 35 are rejected under 35 U.S.C. § 102(e) as being unpatentable over Kuroda (U.S. Patent No. 6,522,608). Claims 3-5, 9-11, 16-18, 25-27, and 32-34

are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kuroda in view of Vishakadatta et al. (U.S. Pat. No. 6,111,712). Claims 21, 22, 37, and 38 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Kuroda in view of Uno (U.S. Pat. No. 6,301,066).

SUMMARY OF CLAIMED SUBJECT MATTER

Independent claim 1 recites a read circuit that provides multi-bit disk data to a disk controller based on analog data from a disk head. The read circuit includes a bit detector for providing single bit digital data that corresponds to the analog data from the disk head. A synchronization mark detector detects a synchronization marker in response to the bit detector. Independent claims 8, 14, 23, and 30 recite similar subject matter. For example, claim 8 recites detecting single bit digital data that corresponds to analog data from the disk head, and detecting a synchronization mark based on the single bit digital data. Claim 14 recites bit detector means for providing single bit digital data corresponding to the analog data from the disk head and synchronization mark detector means for detecting a synchronization maker in response to the single bit digital data. Claim 23 recites a bit detector for providing single bit digital data corresponding to the analog data from the disk head and a synchronization mark detector for detecting a synchronization marker in response to the bit detector. Claim 30 recites bit detector means for providing single bit digital data corresponding to the analog data from the disk head and synchronization mark detector means for detecting a synchronization marker in response to the single bit digital data.

ARGUMENT

Applicant respectfully submits that Kuroda fails to show, teach, or suggest a bit detector for providing single bit digital data corresponding to the analog data from the disk head and a synchronization mark detector for detecting a synchronization maker in response to the bit detector.

Initially, Applicant respectfully submits that Kuroda fails to show, teach, or suggest a bit detector for providing single bit digital data corresponding to the analog data from the disk head. As shown in an exemplary embodiment in FIG. 3, Applicant's read circuit 100 includes a bit detector 114. The bit detector 114 receives digital data from an analog-to-digital converter (ADC) 112. The ADC 112 converts analog data from a disk head 103 (via a pre-amp 102) to digital data. The bit detector 114 receives the digital data and outputs single bit digital data. In other words, the bit detector 114 provides single bit digital data that corresponds to the analog data from the disk head 103.

The Examiner alleges that a PLL circuit 70 shown in FIG. 6 of Kuroda discloses the bit detector as claim 1 recites, because the PLL circuit 70 outputs a synchronizing clock and "it is well known in the art that a clock consists of "1" and "0" bits, hence providing a single data bit." (See Page 2, Lines 16-18 of the Office Action mailed July 27, 2006). Applicant respectfully notes that the alleged single bit digital data output from the PLL circuit 70 does not correspond to the analog data from the disk head.

In contrast, as best understood by Applicant, the PLL circuit 70 outputs a wobble synchronization clock. As shown in FIG. 6, a read signal from a disc 1 is passed through an amplifier 61 and a band pass filter 62 to a wobble detecting circuit 63. The

wobble detecting circuit 63 extracts a wobble signal from the read signal. The PLL circuit 70 generates a wobble synchronization clock based on the wobble signal. As such, the PLL circuit 70 is not a bit detector that provides single bit digital data corresponding to the analog data from the disk head and instead provides a synchronization clock corresponding to a wobble signal.

Even if the PLL circuit 70 provides single bit digital data corresponding to the analog data from the disk head, which Applicant does not concede in view of the above remarks, Applicant respectfully submits that Kuroda fails to show, teach, or suggest a synchronization mark detector for detecting a synchronization marker in response to the bit detector. As shown in FIG. 3, Applicant's read circuit 100 includes a sync mark detector 118. The sync mark detector 118 receives the single bit digital data from the bit detector 114 and detects a synchronization marker in the single bit digital data. In other words, the sync mark detector 118 detects a synchronization marker in response to the bit detector as claim 1 recites.

The Examiner alleges that a sync detecting circuit 69 as shown in FIG. 6 discloses the synchronization mark detector. Applicant respectfully notes that the sync detecting circuit 69 does not detect a synchronization marker **in response to** the alleged bit detector. The sync detecting unit 69 receives an analog read signal from a reproducing amplifier 61. The sync detecting unit 69 detects a synchronization signal in the read signal. As best understood by Applicant, the sync detecting unit 69 does not receive single bit digital data from the alleged bit detector or any other element, and instead responds to analog data received from the reproducing amplifier 61. As such,

Kuroda fails to show, teach, or suggest a synchronization mark detector for detecting a synchronization marker in response to the bit detector.

CONCLUSION

Applicant respectfully submits that Kuroda fails to teach or suggest the limitations of Applicant's claim 1. Kuroda fails to show, teach, or suggest a bit detector for providing single bit digital data corresponding to the analog data from the disk head, and instead discloses a PLL circuit that provides a wobble synchronization clock based on a wobble signal. Kuroda fails to show, teach, or suggest a synchronization mark detector for detecting a synchronization marker in response to the bit detector and instead discloses a sync detecting circuit that detects a synchronization signal in response to an analog read signal from an amplifier. Accordingly, Applicant respectfully submits that claim 1 and the remaining independent claims, as well as their corresponding dependent claims, should be allowable for at least the above reasons.

Respectfully submitted,

Dated: October 23, 2006

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